IN THE CLAIMS:

The status of each claim that has been introduced in the above-referenced application is identified in the ensuing listing of the claims. This listing of the claims replaces all previously submitted claims listings.

1. (Currently amended) A semiconductor device assembly, comprising:

a first semiconductor device including a surface with a plurality of ~~peripherally located~~ bond pads located adjacent to at least three peripheral edges of the surface;

a rerouting element positioned over the first semiconductor device, the rerouting element comprising:

a base substrate;

a plurality of conductive vias positioned adjacent at least ~~two~~ three peripheral edges of the base substrate, each conductive via of the plurality of conductive vias being located so as to align with a corresponding, peripherally located bond pad of the first semiconductor device upon assembly of the rerouting element with the first semiconductor device;

a plurality of conductive traces; and

a plurality of rerouted bond pads located adjacent to another, single edge or two adjacent peripheral edges of the base substrate, each conductive trace of the plurality of conductive traces extending from a corresponding conductive via of the plurality of conductive vias toward the another, single ~~at least one other~~ peripheral edge or the two adjacent peripheral edges of the base substrate to a corresponding rerouted bond pad of the plurality of rerouted bond pads; and

a second semiconductor device positioned over a portion of the rerouting element, each of the plurality of rerouted bond pads being exposed beyond a periphery of the rerouting element.

2. (Previously Presented) The semiconductor device assembly of claim 1, wherein each rerouted bond pad of the plurality of rerouted bond pads is located laterally adjacent a periphery of the first semiconductor device.

3. (Previously Presented) The semiconductor device assembly of claim 1, wherein each rerouted bond pad of the plurality of rerouted bond pads is located adjacent a single edge of the first semiconductor device.

4. (Original) The semiconductor device assembly of claim 1, further comprising: a carrier substrate.

5. (Previously Presented) The semiconductor device assembly of claim 4, wherein the first semiconductor device is secured to the carrier substrate.

6. (Previously Presented) The semiconductor device assembly of claim 4, wherein the carrier substrate comprises at least one of a circuit board, an interposer, another semiconductor device, and leads.

7. (Previously Presented) The semiconductor device assembly of claim 4, wherein the at least one rerouted bond pad is in communication with a corresponding contact area of the carrier substrate.

8. (Previously Presented) The semiconductor device assembly of claim 7, further comprising:
a discrete conductive element positioned between the at least one rerouted bond pad and the corresponding contact area.

9. (Previously Presented) The semiconductor device assembly of claim 8, wherein the discrete conductive element comprises at least one of a bond wire, a tape-automated bond element trace, and a lead.

10. (Previously Presented) The semiconductor device assembly of claim 1, further comprising:
another rerouting element on a bond pad-bearing surface of the second semiconductor device.

11. (Previously Presented) The semiconductor device assembly of claim 1, wherein the second semiconductor device is oriented in staggered relation to the first semiconductor device.

12. (Previously Presented) The semiconductor device assembly of claim 1, wherein the second semiconductor device is smaller than the first semiconductor device.

13. (Previously Presented) The semiconductor device assembly of claim 1, further comprising:
at least one additional semiconductor device positioned over the second semiconductor device.

14. (Previously Presented) The semiconductor device assembly of claim 8, further comprising:
an encapsulant protecting at least portions of the first semiconductor device, the second semiconductor device, the discrete conductive element, and portions of the carrier substrate located laterally adjacent outer peripheries of the first and second semiconductor devices.

15. (Previously Presented) The semiconductor device assembly of claim 14, wherein the encapsulant comprises a glob-top type encapsulant.

16. (Previously Presented) The semiconductor device assembly of claim 14, wherein the encapsulant comprises a transfer molding compound.

17. (Previously Presented) The semiconductor device assembly of claim 14, further comprising:

at least one external connective element in communication with at least one bond pad of the first semiconductor device.

18. (Currently amended) A rerouting element for use with a semiconductor device, comprising:

a base substrate;

a plurality of conductive vias positioned adjacent at least ~~two~~ three peripheral edges of the base substrate, each conductive via of the plurality of conductive vias being located so as to align with a corresponding, peripherally located bond pad of the semiconductor device upon assembly of the rerouting element with the semiconductor device;

a plurality of conductive traces; and

a plurality of contact pads located adjacent to another, single edge or two adjacent peripheral edges of the base substrate, each conductive trace of the plurality of conductive traces extending from a corresponding conductive via toward ~~at least one other~~ the another single peripheral edge or the two adjacent peripheral edges of the base substrate to a corresponding contact pad of the plurality of contact pads.

19. (Previously Presented) The rerouting element of claim 18, wherein the plurality of conductive vias are positioned adjacent three peripheral edges of the base substrate.

20. (Previously Presented) The rerouting element of claim 19, wherein each contact pad of the plurality of contact pads is positioned adjacent to another, single peripheral edge of the base substrate.

21. (Previously Presented) The rerouting element of claim 18, wherein the plurality of conductive vias are positioned adjacent to two adjacent peripheral edges of the base substrate.

22. (Previously Presented) The rerouting element of claim 21, wherein each contact pad of the plurality of contact pads is positioned adjacent to at least one of two other adjacent peripheral edges of the base substrate.